In the Claims:

1-2. (cancelled)

3. (new) A process of selecting TAP connections in an integrated circuit having plural cores with each core having a TAP, each TAP is coupled to a TLM, which selects one of the TAPs, and the TAPs and TLM operating in accordance with the IEEE 1149.1 test interface, comprising:

A. performing an IEEE 1149.1 instruction scan operation with a TAP instruction augmented with a TLM scan code;

B. performing an IEEE 1149.1 data scan operation with TAP selection data to load the TLM with new TAP selection information; and

C. performing IEEE 1149.1 instruction and data scan operations on the TAP selected with the new TAP selection information.

4. (new) The process of claim 3 in which the performing an IEEE 1149.1 instruction scan operation with a TAP instruction augmented with a TLM scan code includes scanning the TLM scan code through an instruction register of a TAP and then into the TLM.

5. (new) The process of claim 3 in which the performing an IEEE 1149.1 instruction scan operation with a TAP instruction augmented with a TLM scan code includes scanning the TLM scan code through an instruction register of a TAP and then into an augmentation instruction shift register in the TLM.

6. (new) The process of claim 3 in which the performing an IEEE 1149.1 instruction scan operation with a TAP instruction augmented with a TAP scan code includes

maintaining IEEE 1149.1 instruction and data scan operations on the TAP selected with the new TAP selection information.

7. (new) The process of claim 3 in which the performing an IEEE 1149.1 instruction scan operation with a TAP instruction augmented with a TLM scan code includes performing an instruction register update, disabling scan access to the currently selected TAP, and enabling the performing an IEEE 1149.1 data scan operation with TAP selection data to load the TLM with new TAP selection information